




SPECIFICATION SHEET

SPECIFICATION SHEET NO.	R0722- 1812B103K202MK	
DATE	Jul. 22, 2024	
REVISION	A3	Updated With Most Recent Data
DESCRIPTION AND MAIN PARAMETRICS	<p>Multilayer Ceramic Chip Capacitors 1812 (4532 Metric) Series, High Voltage, L4.50*W3.20*H2.50mm, Thickness: 2.80mm Max. Dielectric X7R, Capacitance 10nF, Tolerance $\pm 10\%$, Rated Voltage 2000V Operating Temp. Range -55° C ~+125° C Package in Tape/Reel, 500pcs/Reel RoHS/RoHS III compliant</p>	
CUSTOMER		
CUSTOMER PART NO.		
CROSS REF. PART NO.		
ORIGINAL MFG/PART NO.	Aillen/1812B103K202MK-G	
PART CODE	1812B103K202MK	

VENDOR APPROVE			
Issued/Checked/Approved			
DATE: Jul. 22, 2024			

CUSTOMER APPROVE	
DATE:	

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

DESCRIPTION

MLCC consists of a conducting material and electrodes. To manufacture a chip-type SMT and achieve miniaturization, high density and high efficiency, ceramic condensers are used. MLCC is made by NPO, X7R, and Y5V dielectric material and which provides medium Voltage product with high electrical precision, stability and reliability.

MAIN FEATURE

- RoHS III Compliant
- Wide Operating Temperature Range -55~+125°C
- High Capacitance and High Voltage In Given Case Size
- A Wide Selection Of Sizes Is Available (0805 to 1812)
- Capacitor With Lead-free Termination (Pure Tin)



APPLICATION

- DC to DC converter
- High voltage coupling/DC blocking
- Back-lighting inverters
- Snubbers in high frequency power converters

HOW TO ORDER

- Please indicate part code OR custom parameters code and send us your RFQ by E-mail

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

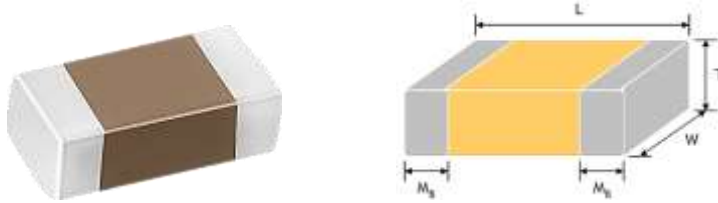
PART CODE GUIDE

RFQ
Request For Quotation

CODE	NAME	KEY SPECIFICATION OPTION
1812	Size	0805 (2012): L2.00*W1.25mm; 1206 (3216) :L3.20*W1.60mm 1210 (3225): L3.20*W2.50mm; 1808 (4520) :L4.50*W2.00mm 1812 (4532): L4.50*W3.20mm;
B	Dielectric	N: NPO (COG); B: X7R; Y: Y5V;
103	Capacitance	Two significant digits followed by number of Zero, The 3rd digit signifies the multiplying factor, and letter R is decimal point. 0R5: 0.5pF; 101: 100pF; 471: 470pF; 103: 10nF; 330: 33pF
K	Tolerance	B=±0.1pF; C=±0.25pF; D=±0.5pF; F=±1%; G=±2%; J=±5%; K=±10%; M=±20%
202	Rated Voltage	Two significant digits followed by No. of zeros. "R" is in place of decimal point. 102=1000 VDC; 202=2000 VDC; 302=3000 VDC
M	Thickness	A: 0.60 ± 0.10mm; B: 0.80 ± 0.10mm; C: 0.95 ± 0.10mm; D: 1.25 ± 0.10mm; G: 1.60 ± 0.20mm; I: 1.25 ± 0.20mm; K: 2.00 ± 0.20mm; M: 2.50 ± 0.30mm; N: 0.50+0.05mm; P: 1.60+0.30/-0.10mm; U: 2.80 ± 0.30mm
K	Package	K: 0.5 Kpcs/Reel; A: 1Kpcs/Reel; B: 2Kpcs/Reel; C: 3Kpcs/Reel; D: 4Kpcs/Reel; I: 10Kpcs/Reel; F: others
()	Internal Control	Internal Code: Letter + Number; Blank: N/A;

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES
DIMENSION (Unit: mm)

Image for reference


Table 1

Size Code	L	W	T (Symbol)	Remark	M B
0805(2012)	2.00 ± 0.15	1.25 ± 0.10	0.60 ± 0.10 (A); 0.80 ± 0.10 (B)		0.50 ± 0.20
	2.00 ± 0.15	1.25 ± 0.10	1.25 ± 0.10 (D)	#	
	2.00 ± 0.20	1.25 ± 0.20	1.25 ± 0.20 (I)	#	
1206(3216)	3.20 ± 0.15	1.60 ± 0.15	0.80 ± 0.10 (B)		0.60 ± 0.20 $(0.50 \pm 0.25)^*$
	3.20 ± 0.15	1.60 ± 0.15	0.95 ± 0.10 (C); 1.25 ± 0.10 (D)	#	
	3.20 ± 0.20	1.60 ± 0.20	1.60 ± 0.20 (G);	#	
	$3.20+0.3/-0.1$	$1.60+0.3/0.1$	$1.60+0.3/-0.1$ (P)	#	
1210(3225)	3.20 ± 0.30	2.50 ± 0.20	0.95 ± 0.10 (C) ; 1.25 ± 0.10 (D);	#	0.75 ± 0.25
	3.20 ± 0.40	2.50 ± 0.30	1.60 ± 0.20 (G) ; 2.00 ± 0.20 (K); 2.50 ± 0.30 (M) ;	#	
	$3.20 \pm 0.60^{**}$	$2.50 \pm 0.50^{**}$	2.50 ± 0.50 (M)	#	
1808(4520)	$4.50+0.5/-0.3$	2.03 ± 0.25	1.25 ± 0.10 (D) ; 1.60 ± 0.20 (G); 2.00 ± 0.20 (K) ;	#	0.50 ± 0.25
1812(4532)	$4.50+0.5/-0.3$	3.20 ± 0.30	1.25 ± 0.10 (D); 1.60 ± 0.20 (G); 2.00 ± 0.20 (K);	#	0.50 ± 0.25
	$4.50+0.5/-0.3$	3.20 ± 0.40	2.50 ± 0.30 (M) ; 2.80 ± 0.30 (U)	#	

Reflow soldering only is recommended.

 * For $1206 \geq 1000V \sim 3000V$ products.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES
GENERAL ELECTRONICAL CHARACTERISTICS
Table 2

Dielectric	NPO	X7R
Size	0805, 1206, 1210, 1808, 1812	
Capacitance range*	0.1pF to 0.022μF	100pF to 1.0μF
Capacitance Tolerance	Cap. ≤5pF: C (±0.25pF) 5pF < Cap < 10pF: D (±0.5pF) Cap ≥ 10pF: F (±1%), G (±2%), J (±5%), K (±10%)	J (±5%) #1 K (±10%), M (±20%)
Rated Voltage	1000V to 4000V	
Q/DF*	Cap < 30pF: Cap ≥ 400+20C Cap ≥ 30pF: Q ≥ 1000	DF ≤ 2.5%
Insulation resistance at Ur**	Ur = 1000~3000V: ≥ 10GΩ	
Dielectric strength	1000~3000V: ≥ 1.2 x WVDC 4000: ≥ 1.1 x WVDC	
Operating Temperature	-55 ~ +125°C	
Capacitance Characteristic	±30ppm	±15%
Termination	Ni/Sn (lead-free termination)	

Note:

- X7R products can provide optional J (±5%) capacitance tolerance.* Measured at the condition of 30~70% related humidity.
- NPO: Apply 1.0±0.2Vrms, 1.0MHz±10% for Cap ≤ 1000pF and 1.0±0.2Vrms, 1.0kHz±10% for Cap > 1000pF, 25°C at ambient temperature.
- X7R, X5R: Apply 1.0±0.2Vrms, 1.0kHz±10%, at 25°C ambient temperature.
- Preconditioning for Class II MLCC: Perform a heat treatment at 150 ± 10° C for 1 hour, then leave in ambient condition for 24 ± 2 hours before measurement.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-A

Size	0805	1206			1210		
VDC (V)	1000	1000	1500	2000	1000	1500	2000
0.5pF (0R5)	D						
1.0pF (1R0)	D						
1.2pF (1R2)	D						
1.5pF (1R5)	D	B	B	B			
1.8pF (1R8)	D	B	B	B			
2.0pF (2R0)	D	B	B	B			
2.2pF (2R2)	D	B	B	B			
2.7pF (2R7)	D	B	B	B			
3.3pF (3R3)	D	B	B	B			
3.9pF (3R9)	D	B	B	B			
4.7pF (4R7)	D	B	B	B			
5.6pF (5R6)	D	B	B	B			
6.8pF (6R8)	D	B	B	B			
8.2pF (8R2)	D	B	B	B			
10pF (100)	D	B	B	B	C	C	C
12pF (120)	D	B	B	B	C	C	C
15pF (150)	D	B	B	B	C	C	C
18pF (180)	D	B	B	B	C	C	C
22pF (220)	D	B	B	B	C	C	C
27pF (270)	D	B	B	B	C	C	C
33pF (330)	D	B	C	C	C	C	C
39pF (390)	D	B	C	C	C	C	C
47pF (470)	D	B	C	C	C	C	C
56pF (560)	D	B	D	D	C	D	D
68pF (680)	D	B	D	D	C	D	D
82pF (820)	D	B	D	D	C	D	D
100pF (101)	D	B	D	D	D	D	D
120pF (121)	D	D	G	G	D	D	D
150pF (151)	D	D	G	G	D	G	G
180pF (181)	D	G	G	G	D	G	G

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-B

Size	0805	1206			1210		
VDC (V)	1000	1000	1500	2000	1000	1500	2000
220pF (221)	D	G	G	G	G	G	G
270pF (271)	D	G	P	P	G	K	K
330pF (331)	D	G	P	P	G	K	K
390pF (391)	D	G	P	P	G	M	M
470pF (471)		G			G	M	M
560pF (561)		G			G		
680pF (681)		G			G		
820pF (821)		G			G		
1,000pF (102)		G			G		
1,200pF (122)		G			K		
1,500pF (152)		G			K		
1,800pF (182)		G			K		
2,200pF (222)		G			K		
2,700pF (272)		G			K		
3,300pF (332)		G			K		
3,900pF (392)		G			K		
4,700pF (472)		G			K		
5,600pF (562)					K		
6,800pF (682)					K		
8,200pF (822)					K		
0.010μF (103)					M		
0.012μF (123)					M		
0.015μF (153)					M		
0.018μF (183)					M		
0.022μF (223)					M		

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE - NPO DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-C

Size	1808					1812				
VDC (V)	1000	1500	2000	3000	4000	1000	1500	2000	3000	4000
2.0pF (2R0)	D	D	D	D						
2.2pF (2R2)	D	D	D	D						
2.7pF (2R7)	D	D	D	D						
3.3pF (3R3)	D	D	D	D						
3.9pF (3R9)	D	D	D	D						
4.7pF (4R7)	D	D	D	D						
5.6pF (5R6)	D	D	D	D						
6.8pF (6R8)	D	D	D	D						
8.2pF (8R2)	D	D	D	D						
10pF (100)	D	D	D	D	D	D	D	D	D	D
12pF (120)	D	D	D	D	D	D	D	D	D	D
15pF (150)	D	D	D	D	D	D	D	D	D	D
18pF (180)	D	D	D	D	D	D	D	D	D	D
22pF (220)	D	D	D	D	G	D	D	D	D	D
27pF (270)	D	D	D	D	G	D	D	D	D	D
33pF (330)	D	D	D	D		D	D	D	D	
39pF (390)	D	D	D	D		D	D	D	D	
47pF (470)	D	D	D	D		D	D	D	D	
56pF (560)	D	D	D	D		D	D	D	D	
68pF (680)	D	D	D	D		D	D	D	D	
82pF (820)	D	D	D	D		D	D	D	D	
100pF (101)	D	D	D	K		D	D	D	D	
120pF (121)	D	D	D	K		D	D	D	D	
150pF (151)	D	K	K	K		D	D	D	D	
180pF (181)	D	K	K	K		D	D	D	K	
220pF (221)	D	K	K	K		D	D	D	K	
270pF (271)	K	K	K	K		D	K	K	K	
330pF (331)	K	K	K	K		D	K	K	K	
390pF (391)	K	K	K	K		D	K	K	K	
470pF (471)	K	K	K			K	K	K	K	

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE - NPO DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-D

Size	1808					1812				
VDC (V)	1000	1500	2000	3000	4000	1000	1500	2000	3000	4000
560pF (561)	K	K	K			K	K	K		
680pF (681)	K	K	K			K	K	K		
820pF (821)	K	D	D			K	K	K		
1,000pF (102)	K	G	G			K	K	K		
1,200pF (122)	G	G	G			K				
1,500pF (152)	K	K	K			K				
1,800pF (182)	K	K	K			K				
2,200pF (222)	K	K	K			K				
2,700pF (272)	K					K				
3,300pF (332)	K					K				
3,900pF (392)						M				
4,700pF (472)						M				
5,600pF (562)						M				

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 4-A

Size	0805	1206				1210		
VDC (V)	1000	1000	1500	2000	2500	1000	1500	2000
100pF (101)	B	D	D	D	D	D	D	D
120pF (121)	B	D	D	D	D	D	D	D
150pF (151)	B	D	D	D	D	D	D	D
180pF (181)	B	D	D	D	D	D	D	D
220pF (221)	B	B	D	B	D	D	D	D
270pF (271)	B	D	D	D	D	D	D	D
330pF (331)	B	D	D	D	D	D	D	D
390pF (391)	B	D	D	D	D	D	D	D
470pF (471)	B	D	D	D	D	D	D	D
560pF (561)	B	D	D	D	D	D	D	D
680pF (681)	B	D	D	D	D	D	D	D
820pF (821)	B	D	D	D	D	D	D	D
1,000pF (102)	B	D	D	D	D	D	D	D

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206, 1210, 1808, 1812 SIZES

Table 4-B

Size	0805	1206				1210		
VDC (V)	1000	1000	1500	2000	2500	1000	1500	2000
1,200pF (122)	B	D	G	G	G	D	M	M
1,500pF (152)	D	D	G	G	G	D	M	M
1,800pF (182)	D	D	G	G	G	D	M	M
2,200pF (222)	D	D	G	G	G	D	M	M
2,700pF (272)	D	D	G	G		D	M	M
3,300pF (332)	D	D	G	G		D	M	M
3,900pF (392)	D	D	G			G	M	M
4,700pF (472)	D	D	G			G	M	M
5,600pF (562)	D	D	G			G	M	M
6,800pF (682)	D	D	G			G	M	M
8,200pF (822)	D	D	G			G	M	M
0.010μF (103)	D	D	G			G	M	
0.012μF (123)		G				G		
0.015μF (153)		G				G		
0.018μF (183)						G		
0.022μF (223)								
0.033μF (333)						G		
0.039μF (393)						K		
0.047μF (473)						M		

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206, 1210, 1808, 1812 SIZES

Table 4-C

Size	1808					1812				
VDC (V)	1000	1500	2000	3000	4000	1000	1500	2000	3000	4000
150pF (151)	D	D	D	D	K					
180pF (181)	D	D	D	D	K					
220pF (221)	D	D	D	D	K					
270pF (271)	D	D	D	D	K	D	D	D	K	K
330pF (331)	D	D	D	K	K	D	D	D	K	K
390pF (391)	D	D	D	K	K	D	D	D	K	K
470pF (471)	D	D	D	K	K	D	D	D	K	K

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206, 1210, 1808, 1812 SIZES

Table 4-D

Size	1808					1812				
VDC (V)	1000	1500	2000	3000	4000	1000	1500	2000	3000	4000
560pF (561)	D	D	D	K	K	D	D	D	K	K
680pF (681)	D	D	D	K	K	D	D	D	K	K
820pF (821)	D	D	D	K	K	D	D	D	K	K
1,000pF (102)	D	K	K	K	K	D	D	D	K	K
1,200pF (122)	D	K	K	K		D	D	D	K	M
1,500pF (152)	D	K	K	K		D	D	D	K	M
1,800pF (182)	D	K	K	K		D	D	D	M	M
2,200pF (222)	D	K	K	K		D	D	D	M	
2,700pF (272)	D	K	K	K		D	D	D	M	
3,300pF (332)	D	K	K	K		D	K	K	M	
3,900pF (392)	D	K	K			D	K	K	M	
4,700pF (472)	D	K	K			D	K	K	M	
5,600pF (562)	K	K	K			D	M	M	M	
6,800pF (682)	K	K	K			D	M	M	M	
8,200pF (822)	K	K	K			D	M	M		
0.010μF (103)	K	K	K			D	M	M		
0.012μF (123)	K					K	M	M		
0.015μF (153)	K					K	M	M		
0.018μF (183)	K					M	M	M		
0.022μF (223)						M	M	M		
0.033μF (333)	K					M				
0.039μF (393)	K					M				
0.047μF (473)	K					M				
0.056μF (563)	K					M				
0.068μF (683)						M				
0.10μF (104)						M				

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements												
Visual and Mechanical	-	* No remarkable defect. * Dimensions to conform to individual spec. sheet.												
Capacitance	* Test temp.: Room Temperature. Class I: COG (NP0)	* Shall not exceed the limits given in the detailed spec.												
Q/D.F (Dissipation Factor)	Cap ≤ 1000pF, 1.0 ± 0.2Vrms, 1MHz ± 10% Cap > 1000pF, 1.0 ± 0.2Vrms, 1KHz ± 10% Class II: (X7R) : 1.0 ± 0.2Vrms, 1KHz ± 10% *Before initial measurement (Class II only): To apply de-aging at 150 C for 1hour then set for 24 ± 2 hours at room temp .	NP0: Cap ≥ 30pF, Q ≥ 1000; Cap < 30pF, Q ≥ 400+20C X7R: ≤ 2.5%												
Dielectric Strength	* To apply voltage: 200V~300V ≥ 2 times VDC 400V~450V ≥ 1.2 times VDC 500V~999V ≥ 1.5 times VDC 1000V~3000V ≥ 1.2 times VDC 4000V ≥ 1.1 times VDC * Duration: 1 to 5 sec. * Charge & discharge current less than 50mA.	* No evidence of damage or flash over during test.												
Insulation Resistance	* Test temp.: Room Temperature. Rated voltage: 200~630V (To apply rated voltage (500V max.) for 60 sec.) * Test temp.: Room Temperature. Rated voltage: ≥ 630V (To apply 500V for 60 sec.)	≥ 10GΩ or RxC ≥ 100Ω-F whichever is smaller												
Temperature Coefficient	With no electrical load. <table border="1" data-bbox="339 1657 833 1839"> <thead> <tr> <th>T.C</th> <th>Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td>NP0</td> <td>-55~125°C at 25°C</td> </tr> <tr> <td>X7R</td> <td>-55~125°C at 25°C</td> </tr> </tbody> </table> *Before initial measurement (Class II only): To apply de-aging at 150° C for 1hour then set for 24 ± 2 hours at room temp	T.C	Temp. (°C)	NP0	-55~125°C at 25°C	X7R	-55~125°C at 25°C	<table border="1" data-bbox="972 1618 1306 1897"> <thead> <tr> <th>T.C</th> <th>Capacitance Change</th> </tr> </thead> <tbody> <tr> <td>NP0</td> <td>Within ±30ppm/°C</td> </tr> <tr> <td>X7R</td> <td>Within ±15%</td> </tr> </tbody> </table>	T.C	Capacitance Change	NP0	Within ±30ppm/°C	X7R	Within ±15%
T.C	Temp. (°C)													
NP0	-55~125°C at 25°C													
X7R	-55~125°C at 25°C													
T.C	Capacitance Change													
NP0	Within ±30ppm/°C													
X7R	Within ±15%													

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements															
Resistance to Soldering Heat	<p>* Solder temperature: $260 \pm 5^\circ \text{C}$</p> <p>* Dipping time: $10 \pm 1 \text{ sec}$</p> <p>* Preheating: $120 \text{ to } 150^\circ \text{C}$ for 1 minute before immerse the capacitor in a eutectic solder.</p> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for $24 \pm 2 \text{ hrs}$ at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for $24 \pm 2 \text{ hrs}$ at room temp.</p>	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within $\pm 2.5\%$ or 0.25pF whichever is larger X7R: within $\pm 7.5\%$;</p> <p>* Q/D.F., I.R. and dielectric strength: To meet initial requirements.</p> <p>* 25% max. leaching on each edge.</p>															
Temperature Cycle	<p>* Conduct the five cycles according to the temperatures and time.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Step</th> <th>Temp. ($^\circ\text{C}$)</th> <th>Time(min)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating temp.+0/-3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>Room temp.</td> <td>2~3</td> </tr> <tr> <td>3</td> <td>Max. operating temp.+3/-0</td> <td>30 ± 3</td> </tr> <tr> <td>4</td> <td>Room temp.</td> <td>2~3</td> </tr> </tbody> </table> <p>* Before initial measurement (Class II only): To apply de-aging 150°C for 1 hour and then set for $24 \pm 2 \text{ hours}$ at room temp.* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hour then set for $24 \pm 2 \text{ hours}$ at room temp .</p>	Step	Temp. ($^\circ\text{C}$)	Time(min)	1	Min. operating temp.+0/-3	30 ± 3	2	Room temp.	2~3	3	Max. operating temp.+3/-0	30 ± 3	4	Room temp.	2~3	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within $\pm 2.5\%$ or 0.25pF whichever is larger X7R: within $\pm 7.5\%$</p> <p>* Q/D.F., I.R. and dielectric strength: To meet initial requirements.</p>
Step	Temp. ($^\circ\text{C}$)	Time(min)															
1	Min. operating temp.+0/-3	30 ± 3															
2	Room temp.	2~3															
3	Max. operating temp.+3/-0	30 ± 3															
4	Room temp.	2~3															
Vibration Resistance	<p>* Vibration frequency: $10 \sim 55 \text{ Hz/min}$.</p> <p>* Total amplitude: 1.5mm * Test time: 6 hours. (Two hours each in three mutually perpendicular directions.)</p> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hour then set for $24 \pm 2 \text{ hours}$ at room temp . *Cap./DF(Q) Measurement to be made after de-aging at 150°C for 1hour then set for $24 \pm 2 \text{ hours}$ at room temp.</p>	<p>* No remarkable damage.</p> <p>* Cap change and Q/D.F.: To meet initial spec.</p>															

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES
RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements
Humidity (Damp Heat) Steady State	*Test temp.: $40 \pm 2^\circ \text{C}$ *Humidity: 90~95% RH *Test time: 500+24/-0 hours. * Before initial measurement (Class II only): To apply de-aging at 150°C for 1hour then set for 24 ± 2 hours at room temp . * Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hour then set for 24 ± 2 hours at room temp .	*No remarkable damage. *Cap change: NP0: within $\pm 5\%$ or $\pm 0.5\text{pF}$ whichever is larger X7R: within $\pm 12.5\%$ *Q/D.F Value: NP0: $\text{Cap} \geq 30\text{pF} : \text{Q} \geq 350$ $10\text{pF} \leq \text{Cap} < 30\text{pF} : \text{Q} \geq 275 + 2.5\text{C}$ $\text{Cap} < 10\text{pF} : \text{Q} \geq 200 + 10\text{C}$; X7R: $\leq 3.0\%$ * I.R.: $\geq 1\text{G}\Omega$ or $\text{RxC} \geq 50\Omega\text{-F}$ whichever is smaller.
Humidity (Damp Heat) Load	*Test temp.: $40 \pm 2^\circ \text{C}$ *Humidity: 90~95% RH *Test time: 500+24/-0 hours. • To apply voltage: rated voltage (Max. 500V) *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hour then set for 24 ± 2 hours at room temp . * Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hour then set for 24 ± 2 hours at room temp .	* No remarkable damage. *Cap change: NP0: within $\pm 7.5\%$ or $\pm 0.75\text{pF}$ whichever is larger; X7R: within $\pm 12.5\%$ *Q/D.F Value: NP0: $\text{Cap} \geq 30\text{pF} : \text{Q} \geq 200$; $\text{Cap} < 30\text{pF} : \text{Q} \geq 100 + 10/3\text{C}$ X7R: $\leq 3.0\%$ * I.R.: $\geq 500\text{M}\Omega$ or $\text{RxC} \geq 25\Omega\text{-F}$ whichever is smaller.
Bending Test	* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1 mm per second until the deflection becomes 1 mm and then the pressure shall be maintained for 5 ± 1 sec. *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hour then set for 24 ± 2 hours at room temp . * Measurement to be made after keeping at room temp. for 24 ± 2 hours.	* No remarkable damage. * Cap change: NP0: within $\pm 5.0\%$ or $\pm 0.5\text{pF}$ whichever is larger ; X7R: within $\pm 12.5\%$ (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test.)
Solderability	* Solder temperature: $235 \pm 5^\circ \text{C}$ * Dipping time: 2 ± 0.5 sec.	95% min. coverage of all metalized area

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements
High Temperature Load (Endurance)	<p>* Test temp.: NP0, X7R: $125 \pm 3^{\circ}$ C</p> <p>* To apply voltage:</p> <p>(1) 1206/NP0 (3kV) $\geq 1.5\text{pF}$: 100% of rated voltage. 1812N472&1812N562(1KV): 100% of rated voltage.</p> <p>(2) 200V~300V: 200% of rated voltage.</p> <p>(3) 400V~450V: 120% of rated voltage.</p> <p>(4) 500V: 150% of rated voltage.</p> <p>(5) 630V~3000V: 120% of rated voltage.</p> <p>(6) 4000V: 110% of rated voltage.</p> <p>* Test time: 1000+24/-0 hours.</p> <p>*Before initial measurement (Class II only): To apply de-aging at 150° C for 1hr then set for 24 ± 2 hours at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150° C for 1hour then set for 24 ± 2 hours at room temp.</p>	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within $\pm 3.0\%$ or $\pm 0.3\text{pF}$ whichever is larger. X7R: within $\pm 12.5\%$</p> <p>* Q/D.F. value: NP0: $\text{Cap} \geq 30\text{pF}$, $Q \geq 350$ $10\text{pF} \leq \text{Cap} < 30\text{pF}$, $Q \geq 275 + 2.5C$ $\text{Cap} < 10\text{pF}$, $Q \geq 200 + 10C$ X7R: $\leq 3.0\%$</p> <p>* I.R.: $\geq 1\text{G}\Omega$ or $RxC \geq 50\Omega\text{-F}$ whichever is smaller.</p>
Adhesive Strength of Termination	<p>* Pressurizing force: 5N (≤ 0603) and 10N (> 0603)</p> <p>* Test time: 10 ± 1 sec.</p>	<p>* No remarkable damage or removal of the terminations.</p>

* "Room condition" Temperature: 15 to 35° C, Relative humidity: 25 to 75%, Atmospheric pressure: 86 to 106kPa.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

RECOMMENDED SOLDERING CONDITIONS

The lead-free termination MLCCs are not only to be used on SMT against lead-free solder paste, but also suitable against lead-containing solder paste. If the optimized solder joint is requested, increasing soldering time, temperature and concentration of N2 within oven are recommended.

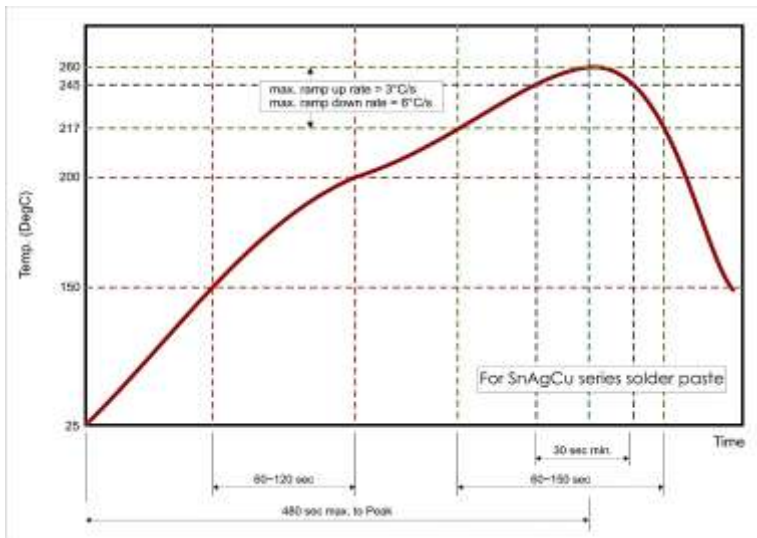


Fig. 1 Recommended reflow soldering profile for SMT process with SnAgCu series solder paste.

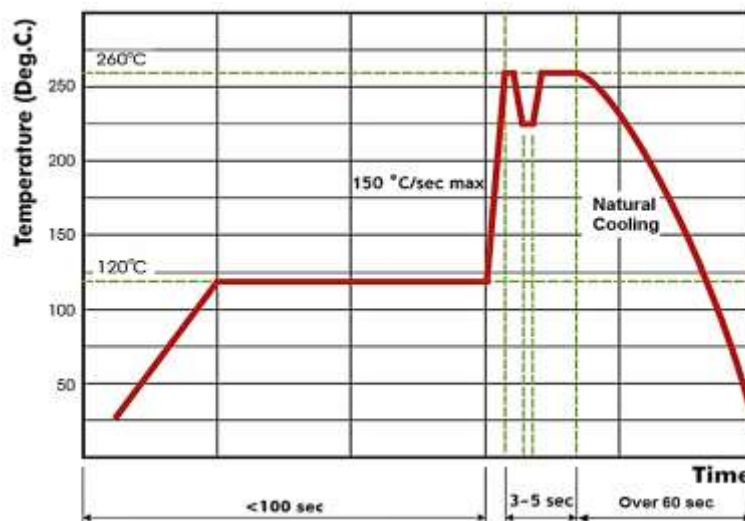


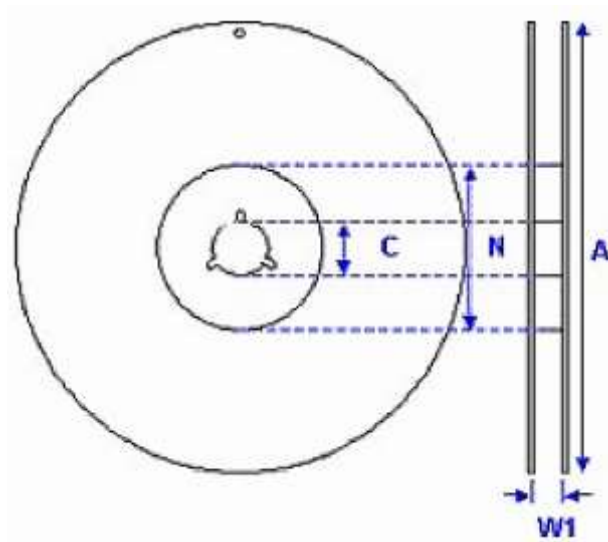
Fig. 2 Recommended wave soldering profile for SMT process with SnAgCu series solder.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES
PACKAGING STYLE AND QUANTITY

Size	Thickness (Symbol)		Paper Tape		Plastic Tape	
			7" Reel	13" Reel	7" Reel	13" Reel
0805 (2012)	0.60±0.10	A	4,000	15,000	-	-
	0.80±0.10	B	4,000	15,000	-	-
	1.25±0.10	D	-	-	3K	10K
	1.25±0.20	I	-	-	3K	10K
1206 (3216)	0.80±0.10	B	4,000	15,000	-	-
	0.95±0.10	C	-	-	3,000	10,000
	1.25±0.10	D	-	-	3,000	10,000
	1.60±0.20	G	-	-	2,000	10,000
	1.60+0.30/-0.10	P	-	-	2,000	9,000
1210 (3225)	0.95±0.10	C	-	-	3,000	10,000
	1.25±0.10	D	-	-	3,000	10,000
	1.60±0.20	G	-	-	2,000	-
	2.00±0.20	K	-	-	1,000	6,000
	2.50±0.30	M	-	-	1,000	6,000
1808 (4520)	1.25±0.10	D			2,000	10,000
	1.60±0.20	G			2,000	8,000
	2.00±0.20	K			1,000	6,000
1812 (4532)	1.25±0.10	D			1,000	5,000
	1.60±0.20	G			1,000	-
	2.00±0.20	K			1,000	-
	2.50±0.30	M			500	3,000

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

REEL DIMENSION (Unit: mm)

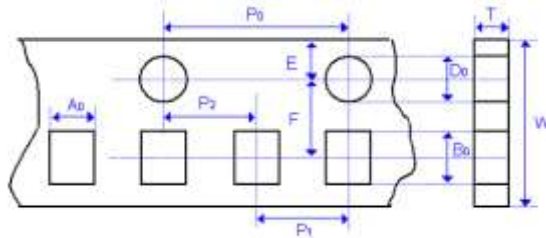


Size Code	0805, 1206, 1210, 1812			1808, 1812
Reel Size	7"	10"	13"	7"
C	13.0±0.5	13.0±0.5	13.0±0.5	13.0±0.5
W 1	10.0±1.5	10.0±1.5	10.0±1.5	12.4+2.0/-0
A	178.0±2.0	250.0±2.0	330.0±2.0	178.0±2.0
N	60.0+1.0/-0	50 min	50 min	60.0+1.0/-0

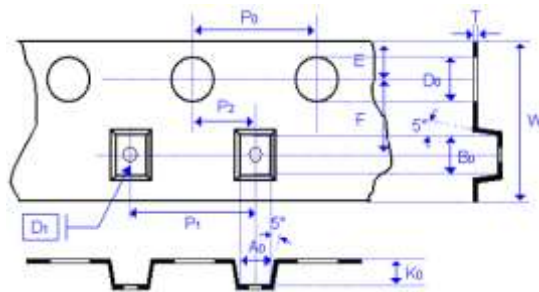
MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

TAPE DIMENSION (Unit: mm)

Paper Tape



Plastic Tape



Size	0805		
Thickness	A, H	B, T	D, I
A0	1.50 ± 0.20	1.50 ± 0.20	< 1.80
B0	2.30 ± 0.20	2.30 ± 0.20	< 2.70
T	≤ 1.15	≤ 1.20	0.23 ± 0.1
K0	-	-	< 2.00
W	8.00 ± 0.30	8.00 ± 0.30	8.00 ± 0.30
P0	4.00 ± 0.10	4.00 ± 0.10	4.00 ± 0.10
10xP0	40.00 ± 0.20	40.00 ± 0.20	40.00 ± 0.20
P1	4.00 ± 0.10	4.00 ± 0.10	4.00 ± 0.10
P2	2.00 ± 0.05	2.00 ± 0.05	2.00 ± 0.05
D0	1.50 + 0.1 / - 0	1.50 + 0.1 / - 0	1.50 + 0.1 / - 0
D1	-	-	1.00 + / - 0.10
E	1.75 ± 0.10	1.75 ± 0.10	1.75 ± 0.10
F	3.50 ± 0.05	3.50 ± 0.05	3.50 ± 0.05

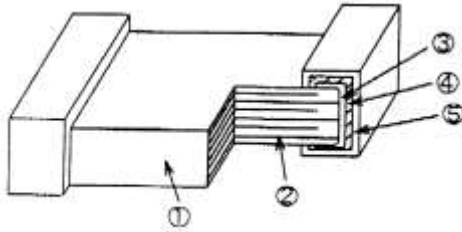
MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES
TAPE DIMENSION (Unit: mm)

Size	1206			1210			
	B, T	C, J, D	G, P	T	C, D	G, K	M
A0	1.90±0.50	< 2.00	<2.30	< 3.05	< 3.05	< 3.05	< 3.20
B0	3.50±0.50	< 3.70	< 4.00	< 3.80	< 3.80	< 3.80	<4.00
T	≤1.20	0.23±0.1	0.23±0.1	0.23±0.1	0.23±0.1	0.23±0.1	0.23±0.1
K0	-	< 2.00	< 2.50	< 1.50	< 2.00	< 2.50	< 3.20
W	8.00±0.30	8.00±0.30	8.00±0.30	8.00±0.30	8.00±0.30	8.00±0.30	8.00±0.30
P0	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
10xP0	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20
P1	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
P2	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05
D0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0
D1	-	1.00±0.10	1.00±0.10	1.00±0.10	1.00±-0.10	1.00±0.10	1.00±0.10
E	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
F	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05

Size	1808		1812		
	D, F	G, K	D, F	G, K	M, U
A0	< 2.50	< 2.50	< 3.90	< 3.90	< 3.90
B0	< 5.30	< 5.30	< 5.30	< 5.30	< 5.30
T	0.25±0.1	0.25±0.1	0.25±0.1	0.25±0.1	0.25±0.1
K0	< 2.00	< 2.50	< 2.00	< 2.50	< 3.50
W	12.00±0.30	12.00±0.30	12.00±0.30	12.00±0.30	12.00±0.30
P0	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
10xP0	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20	40.00±0.20
P1	4.00±0.10	4.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10
P2	2.00±0.10	2.00±0.10	2.00±0.10	2.00±0.10	2.00±0.10
D0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0	1.50+0.1/-0
D1	1.50+/-0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10
E	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
F	5.50±0.10	5.50±0.10	5.50±0.10	5.50±0.10	5.50±0.10

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

Constructions



NO.	Name	NPO	X7R
1	Ceramic material	CaZrO based	BaTiO based
2	Inner electrode	Ni	
3	Termination	Inner electrode	Cu
4		Middle layer	Ni
5		Outer layer	Sn

STORAGE AND HANDLING CONDITIONS

- To store products at 5 to 40°C ambient temperature and 20 to 70% related humidity conditions.
- The product is recommended to be used within one year after shipment. Check solder ability in case of shelf life extension is needed.
- Don't open the tape until the parts are to be used, use the chips within 3 months after the tape is opened.
- For product of high dielectric constant (Class2&3, characteristics B/W & Y), the Electro static capacity changes with the passage of time due to the inherent characteristics of ceramic dielectric materials. The changed capacity reverts to nominal at the temperature it reaches during the soldering process.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

CAUTIONS

- The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solder ability. Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)
- In corrosive atmosphere, solder ability might be degraded, and silver migration might occur to cause low reliability.
- Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sun light, the solder ability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

ROHS COMPLIANCE

- The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU RoHS Directive (EU) 2015/863 EC (RoHS3). RoHS Test Report for this product can be obtained can be obtained at Download Center.

REACH COMPLIANCE

- REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, REACH Test Report for this product can be obtained can be obtained at Download Center.

MULTILAYER CERAMIC CHIP CAPACITORS 1812 SERIES

IMPORTANT NOTES AND DISCLAIMER

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